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SE-8087

B. E. II (Sem. III) (Ele.) Examination

May / June – 2011

Analog & Digital Electronics

(New Course)

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :
☛ **B. E. 2 (Sem. 3) (Ele.)**

Name of the Subject :
☛ **Analog and Digital Electronics**

☛ Subject Code No. : **8 0 8 7** ☛ Section No. (1, 2,.....) : **Nil**

Seat No. :

Student's Signature

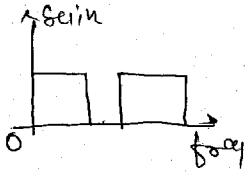
(2) Attempt all the questions.
(3) Figures to right indicate full marks.
(4) Programmable calculators are not allowed.

1 (a) Attempt the following : **10**

(i) _____ is defined as the ratio of differential gain (Ad) and common mode gain (AC)

(ii) For log amplifier _____ device is used as feedback element.

(iii) For inverting adder all the I/Ps to be applied at _____ I/P terminal.

(iv) 

this is the graph of _____ filter.

(v) In the open loop OPAMP configuration has _____ feedback.

(vi) A _____ filter is used for attenuating the low frequency and pass the high frequency.

(vii) _____ is the fixed -ve voltage regulator series.

(viii) IC 7805 given _____ amount of fixed power supply.

(ix) IC 555 is a _____ pin N/P IC

(x) A monostable multivibrator has _____ stable state.

(b) For a monostable multivibrator, the external components are RA = 15 kΩ and C = 0.1 μf. Calculate the ON tince of the load voltage waveform. **2**

(c) Design a monostable multivibrator using IC 555 for VCC = 12 V and pulse width of I m sec. C = 0.1 μf. **3**

(d) Attempt any **one** : **5**

(i) Explain merits and demerits of active filters over passive filters.

(ii) Explain with wave form and circuit, inverting schmitt trigger.

2 (a) Attempt any **two** : **10**

(i) Derive the equation $V_0 = -1/R_1C_f \int_0^t V_{indt} + C$ usingIC 741,

(ii) Explain basic differentiator using OPAMP.

(iii) Explain basic Antilog Amplifier using (diode) and OPAM and derive the equation for that.

(b) Determine the slow rate of a frequency compensated OP AMP at room temperature which has a units cross-over frequency of 5 MHz. **5**

3 Attempt any **three** : **15**

(i) Explain basic PLL operation

(ii) Explain an astable multivibrator using IC 555.

(iii) Explain pulse structure using IC 555.

(iv) Positive peak netator using OPAMP.

4 (a) Mark true or false : **5**

(i) When $\overline{J=1}$ and K=1 the flip flop does not toggles.

(ii) When $\overline{CLR}$=0, the clock input does not have any effect on flip flop.

(iii) In master slave flip flop the length of the time required for its output to change state equals the width of one clock pulse.

(iv) Flip flop may be used to divide the input frequency by any number.

(v) N flip flop can count up to 2^N pulses.

(b) Explain below terms : **5**

(i) Lock out problem

(ii) Race around condition

(c) Answer the following : **10**

(i) Quadruple 2 to 1 line multiplexer could be made by
  (a) 8 Nand and 3 OR gate
  (b) 4 Nand and 4 OR gate
  (c) 8 Nand and 4 OR gate
  (d) None of the above

(ii) _____ is a digital function that has 2^n or less input lines and n output lines.
  (a) Multiplexer
  (b) demultiplexer
  (c) encoder
  (d) Decoder

(iii) _____ means transmitting a large number of information units over a smaller number of channels or lines.
  (a) Multiplexer
  (b) Demultiplexer
  (c) Encoder
  (d) Decoder

(iv) _____ enumerates the time sequence of inputs, outputs and flip flop states to gather
  (a) Truth table
  (b) Excitation table
  (c) State table
  (d) None of the above

(v) State equation is also known as _____
  (a) Boolean equation
  (b) state algebra
  (c) application equation

(vi) _____ is the technique where the number of flip flop can be reduced.
  (a) Tabulation method
  (b) State reduction
  (c) K'map

(vii) _____ Circuit does not include memory element.
  (a) Sequential circuit
  (b) Combinational circuit
  (c) both

(viii) In JK flip flop when both inputs are 1 the output will be
  (a) Q (t)
  (b) Q' (t)
  (c) None of them

(ix) _____ flip flop receives the designation from its ability to transfer data into a flip flop. It is basically RS flip-flop with an inverter in the R inpujt.
(a) T
(b) JK
(c) D

(x) A sequential circuit that goes through a prescribed sequence of states upon the application of input pulses is called a _____.
(a) Sequence converter
(b) shift register
(c) counter

5 (a) A decimal counter follows a sequence of ten states and returns to 0 after the count of 9. Design this asynchronous counter with different flip-flop transition steps. **7**

(b) Design a type T counter that goes through states 0,3,5,6,0. Is the counter self starting ? **8**

OR

5 (a) Design two-bit ripple up/down counter using positive edge-triggered JK flip flops. **7**

(b) Design a J-K counter that goes through states 3,4,5,6 and 3..... Is the counter self-starting ? **8**

6 Answer any **three** : **15**

(i) 4 bit shift register with parallel load

(ii) Explain clocked Master Slave JK Flip Flop

(iii) Convert SR FF to D FF

(iv) Design a mod-6 asynchronous counter using T FFs.